Atty. Docket No. PIA30746/DBE/US
Serial No: 10/627,057

Remarks

Claim 1 has been amended to attempt to clarify the configuration of the claimed method. Claims 11-14 were previously canceled. Thus, Claims 1-10 are active in the present application.

The present invention relates to a method for fabricating an RF semiconductor device. The method (as set forth in Claim 1) generally comprises:

a) forming a trench to define an active region and an element isolation region in a semiconductor substrate;
b) forming a plurality of gate lines within the active region of the semiconductor substrate, the plurality of gate lines not extending over a center of the trench;
c) forming an insulating layer on the plurality of gate lines and the semiconductor substrate;
d) only one contact-hole-forming step which consists of the step of forming at least one contact hole in the insulating layer within the active region without forming the at least one contact hole within the element isolation region;
e) forming a contact plug in each contact hole; and
f) forming a conductive pattern layer that is electrically connected with the contact plug.

The references cited against the claims clearly and unambiguously form a contact hole in an insulating layer within an element isolation region (see, e.g., the representative drawings on the front/cover pages of Yeh et al. and Ma et al.). Accordingly, the present claims are not anticipated by either cited reference.

Applicant's undersigned representative notes that the present Claim 1 is not intended to exclude the possibility of forming further insulating layers over the conductive pattern layer, or forming contact holes in such further insulating layers. However, in the insulating layer formed

on gate lines and under a conductive pattern layer, contact holes are formed only within the active region, and not within the element isolation region.

The Rejection of Claims 1, 7-8 and 10 under 35 U.S.C. § 102(b)

The rejection of Claims 1, 7-8 and 10 under 35 U.S.C. § 102(b) as being anticipated by Yeh et al. (U.S. Pat. No. 6,294,834) is respectfully traversed.

Yeh et al. clearly disclose a contact hole in an insulating layer within an element isolation region (see, e.g., the representative drawing on the cover page of Yeh et al.). More specifically, Yeh et al. show in FIG. 1 thereof a shallow trench isolation layer 16 formed between SOI substrate 14 and single crystal Si resistor layer 20, and a capacitor 32 on the single crystal Si resistor layer 20, wherein the capacitor 32 is composed of a lower electrode 34, an oxide layer 36 and an upper electrode 38 (see also col. 1, ll. 22-26 and 35-39). A multilevel dielectric layer 40 is formed on the silicon substrate 10 (see col. 1, ll. 47-48). A plurality of via openings 42, 44, 46 and 48 are formed in the dielectric layer 40 (see col. 1, ll. 48-51). The via opening 46 is filled with a multilevel interconnects layer 54, which is electrically connected to the lower electrode 34 of the capacitor 32 (see col. 1, ll. 56-58). The via opening 46 is clearly over STI layer 16 (FIG. 1), which would appear to define an element isolation region of the SOI substrate 14. Accordingly, Yeh et al. do not disclose a method that includes only one contact-hole-forming step in the insulating layer between a plurality of gates and a conductive pattern layer, in which at least one contact hole is formed within the active region and not within the element isolation region.

Therefore, the present claims are not anticipated by Yeh et al. As a result, this ground of rejection is unsustainable, and should be withdrawn.

The Rejection of Claims 1-4, 9 and 11-12 under 35 U.S.C. § 102(b)

The rejection of Claims 1-4, 9 and 11-12 under 35 U.S.C. § 102(b) as being anticipated by Ma et al. (U.S. Pat. No. 5,939,753) is respectfully traversed.

Ma et al. clearly disclose a contact hole in an insulating layer within an element isolation region (see, e.g., the representative drawing on the cover page of Ma et al.). More specifically, Ma et al. show in FIG. 8 thereof a dielectric layer 120 formed between gates 53, 54 and 55 and metallization regions (e.g., 135, 136, 138 and 139, electrically coupled to bottom polysilicon plate 44 and top polysilicon plate 56 of DPC 57, and to electrodes 108 and 109 of polysilicon resistor 58, respectively; see also col. 4, ll. 41-47, and col. 8, ll. 8-28). Top and bottom polysilicon plates 44 and 56 of double polysilicon capacitor (DPC) 57 and polysilicon resistor 58 are formed on field oxide layer 38 (see col. 4, ll. 39-45), which would appear to define an element isolation region. Accordingly, Ma et al. do not disclose a method that includes only one contact-hole-forming step in the insulating layer between a plurality of gates and a conductive pattern layer, in which at least one contact hole is formed within the active region and not within the element isolation region.

Therefore, the present claims are not anticipated by Ma et al. As a result, this ground of rejection is unsustainable, and should be withdrawn.

The Rejection of Claims 5-6 under 35 U.S.C. § 103(a)

The rejection of Claims 5-6 under 35 U.S.C. § 103(a) as being unpatentable over Ma et al. in view of Hsu et al. (U.S. Pat. No. 6,444,517) is respectfully traversed.

As explained above, Ma et al. are saliently deficient with regard to a method that includes only one contact-hole-forming step in the insulating layer between a plurality of gates and a conductive pattern layer, in which at least one contact hole is formed within the active region and not within the element isolation region. Hsu et al. fail to cure this deficiency.

Hsu et al. disclose a high Q inductor with simultaneous Cu damascene via/trench etching (Title). Hsu et al. are silent with regard to gates and gate electrodes. Similarly, Hsu et al. are silent with regard to field oxides, STI structures or processes, and (apparently) isolation regions of any kind. Thus, it is not possible for Hsu et al. to cure the deficiency of Ma et al. with regard to the present Claim 1.

Claims 5-6 depend from Claim 1, and therefore contain all of the limitations of Claim 1. As a result, it is not possible for Hsu et al. to cure the deficiency of Ma et al. with regard to the present Claims 5-6. Therefore, this ground of rejection is unsustainable, and should be withdrawn.

The Objection to Claim 1

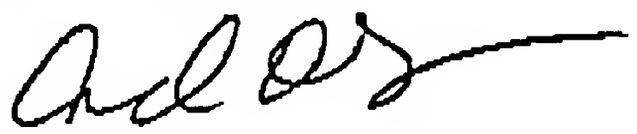
The objection to Claim 1 has been obviated by appropriate amendment.

Conclusions

In view of the attached Declaration and above remarks, all bases for objection and rejection are overcome, and the application is in condition for allowance. Early notice to that effect is earnestly requested.

If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

Respectfully submitted,



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